Low-Power Phase Frequency Detector Using Hybrid AVLS and LECTOR Techniques for Low-Power PLL

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Abstract. *Wireless communication is a fast-growing industry and recent developments focus on improving certain aspects of the area and reducing the power consumption while maintaining the frequency of operation. Phase Locked Loop (PLL) is an integral part of communication circuits which operate at very high frequencies. Phase Frequency Detector (PFD) is the first block of PLL and is key in determining the computational capacity of the PLL. The power consumption of the PFD has to be reduced to minimize the overall power consumption of PLL. The PFD architecture used is based on Double Edged Triggered D Flip-Flop (DET-DFF), which is free of dead zone. Stack, LECTOR, AVLS and hybrid low-power approaches are implemented to reduce the power consumption of DET-DFF based PFD architectures. The PFDs power, delay and power delay product analysis is performed using Cadence Virtuoso and Spectre in CMOS* 180 *nm and* 90 *nm technology. A power reduction of upto* 32 *% has been observed while keeping the transistor count to a minimum.*

Keywords

AVLS, LECTOR, Phase Frequency Detector, Phase Locked Loop, stack.

1. Introduction

Phase Locked Loops (PLL) circuits are used to produce very high frequency periodic signals. The PLL is composed of Phase Frequency Detectors (PFD), a charge pump, a loop filter and Voltage-Controlled Oscillator (VCO) and a frequency divider. PLL works on the principle of negative feedback. An optional amplifier can also be used after the VCO in the case of weak signals. Based on the PFD outputs, the charge pump produces a tuning current which controls the VCO to produce a high frequency periodic signal. The most frequently used applications of PLL are frequency synthesizers, Zigbee modules and high frequency demodulators.

The system level block diagram of PLL is shown in Fig. 1. PFD is the first block and behaves as a bottleneck deciding the overall efficiency of PLL. The input frequency is generated using crystal oscillators [15]. Due to its analog nature, it is prone to noise and interference and this may result in jitter in the output. The phase detector determines phase differences between input and divided clock signal [7].

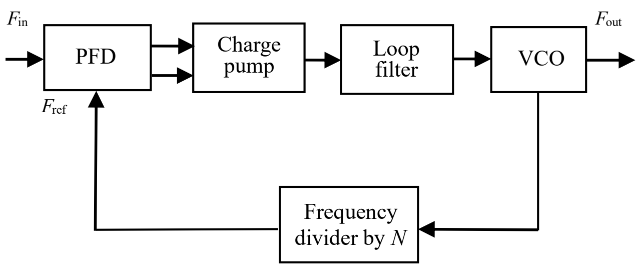

Fig. 1: Block representation of phase locked loop.

PFD produces two (UP and DOWN) outputs based on the reference input and feedback frequency, which is made into a single tuning signal as input to VCO through the loop filter. Another sub-component of PLL is the charge pump which converts the two (UP and DOWN) incoming signals from the PFD into one.

The charge pump output voltage is passed through a loop filter to reduce ripples and provide stability. This filtered signal acts as input to VCO, which gives stable output oscillations. The schematic of the charge pump is shown in Fig. 2.

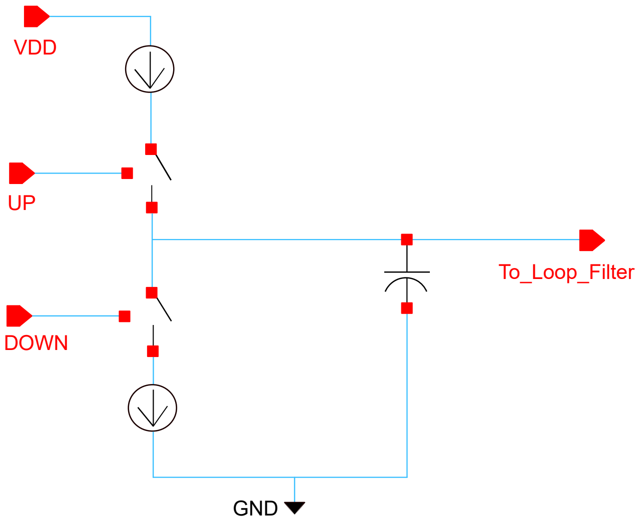

Fig. 2: Schematic of charge pump.

A combination of two DET-DFF is used as PFD. A DET-DFF is considered as it has advantages in terms of power dissipation and computational speed. The outputs UP and DOWN signals are taken from each DFF. When the input data is leading the clock, the UP signal rises and the DOWN signal sees a rising edge when the clock leads the input data. The output remains high until the condition is persistent. The phase difference is represented in Eq. (1):

$$\Delta\text{Ø} = \frac{\Delta t}{T_{\text{ref}}}, \tag{1}$$

where ΔØ is a phase error, Δt is time delay between the peak of two signals and T_{ref} is the time period of input reference signal. Equation (2) shows the output voltage of a PFD (V_{PFD}) in terms of source voltage (V_{DD}) and phase error:

$$V_{\text{PFD}} = \frac{V_{\text{DD}}}{4\pi}\Delta\text{Ø}. \tag{2}$$

Equation (3) denotes the gain of PFD (K_{PFD}) in terms of V$\cdot$rad^{-1}:

$$K_{\text{PFD}} = \frac{V_{\text{DD}}}{4\pi}. \tag{3}$$

Phase error is zero when the PLL is locked. Equation (1), Eq. (2) and Eq. (3) enable calculation of the output parameters of PLL such as phase error, voltage, and gain [1]. Certain conditions must be considered while designing a PFD, such as the maximum variance between feedback and input signal and input transition sensibility, called dead zone and blind zone, respectively. The dead zone goes undetected, and the blind zone can reduce the computational capacity of the PFD. Dead zones can be avoided at the cost of increased complexity of transistor count [3]. There are multiple architectures of PFD.

The PFD can be with and without a dead zone. They are chosen based on their circuit requirements, operational range, noise sensitivity and power [13]. In the present scenario leakage power is a dominant component in Complementary Metal-Oxide-Semiconductor (CMOS) circuits [5]. The total power consumption can be reduced by using low-power architectures such as Adiabatic, LECTOR, Adaptive Voltage Level at Source (AVLS), and stack and hybrid architectures with the combination of two or more techniques.

The objective of the proposed work is to reduce the power consumption of a PFD, which in turn reduces the power consumption of PLL. This is achieved by incorporating predominant low-power techniques such as LECTOR, AVLS, stack and other hybrid approaches as well to DET based PFD. The proposed circuits are realized and simulated in CMOS 180 nm technology using Cadence Virtuoso and Spectre. Power analysis is performed using Cadence Spectre. A supply voltage of a constant 1.8 V was used throughout the work.

The rest of the paper has been organized into sections. Section 2. consists of a literature review of multiple PFD architectures, sub-blocks of PLL and low-power techniques. Design methodology of existing PFD architectures and low-power techniques are discussed under Sec. 3. Simulation results and analysis have been discussed in Sec. 4. Inferences derived from the simulation and analysis and their pros and cons are discussed under Sec. 5.

2. Literature Review

PLL is used widely in communication systems such as Global System for Mobile Communications (GSM) and transceiver circuits [15]. PLL should be very precise with reduced skew time and jitter in synchronization applications with lower locking time. The PLL is implemented in 90 nm technology and has an operational range of 250 to 950 MHz [2]. The objective of this PLL is to attain a high range of capture and low lock in time, which is determined by the architecture of the PFD used.

A DET-DFF architecture has been implemented in [1]. The PFD circuit constructed using this DET is area efficient compared to traditional and conventional PFD circuits in [8] and [9]. The operation of the circuit is as follows: two DFF are used which are always operated at high logic input. The input from the frequency divider acts as negative feedback and the other input is from external data signals. This circuit consumes 4.65 µW of power when operated at an input frequency of 20 MHz.

PLL architecture with a dead zone is discussed in [7]. Introduction of a controlled dead zone reduces the total power consumption. Although PFD is the bottleneck, other components of PLL such as the loop filter, charge pump, frequency divider and VCO can also be fine-tuned to consume less power. Peak to peak jitter is introduced with AVLS and dead zone which should be reduced. This PLL can be used where power is a priority constraint.

A DET-DFF was realized in 130 nm technology for GHz application, using the multiple variable threshold [14]. The circuit consists of nine transistors based on Exclusive OR gate. The approach used here is using transmission gates. Furthermore, inverters were used in back-to-back configuration. A 9.6 % power reduction was observed for a 5 % increase in speed.

An all-digital PLL exclusively used for wireless applications has been developed in [11]. It uses a digital PFD, a digital loop filter and digital VCO by means of a ring oscillator. Multiple stages of the ring oscillator can be used based on the application and the constraints on power and area. The locking period is observed to be 50 ps and a frequency of about 4.7 GHz. Replacing the analog components with digital components reduces the sensitivity of the circuit to noise and interference.

A DET pulse clocked TSPC logic DFF has been discussed in [4]. The circuits simulated show a reduction in speed area power product of upto 63 %. It is specifically designed for high speed and low-power applications. Since the transistor count of the circuit is 8, the area is reduced by 60 % as compared to a conventional DET-DFF.

Two PFD architectures have been discussed [12] in 90 nm technology. It is implemented with a source voltage of 1.8 V. The reset process has been eliminated and both the circuits are free of dead zone. Although both the circuits are high performing with low-power and jitter, a circuit with 8 transistors has lower output capacity compared to others which will require an external amplifier circuit for certain voltage sensitive applications.

Transistor stacking is done in circuits by replacing a transistor with two transistors of the same width and same technology [16]. By introducing another transistor to the path, the leakage current from source to ground when the circuit is unused is reduces by the increased resistance. To increase the transistor stacking effect, the number could be increased more than two and by using a transistor of the appropriate width. They are variants of Stack which has a control transistor named as sleep transistor which turns the circuit into sleep mode. The downside of the stack is the area increases by two-fold.

A hybrid low-power approach involves combining two or more techniques for one application. Many low-power architectures are discussed, such as Adaptive Voltage Level (AVL), adiabatic, LECTOR, stack, clock gating, but all of them cannot be used together with each other for a single application due to their difference in nature of working. Careful analysis must be performed to use two or more techniques. Keeping in mind that the desired result the output must be efficient and should be less complex.

Study has been done on various low-power architectures and hybrid along with their advantages and disadvantages. After reviewing the latest trends in the technology related to PFD and PLL, the work has been proposed with the aim of reduction in power consumption with very minimal area changes.

3. Design and Implementation

The PFD architectures can be designed with and without a dead zone, with and without a reset path and so on. The proposed work uses PFD without dead zone without reset path in power critical applications. The schematic of DET-DFF is shown in Fig. 3. The DET-DFF uses True Single-Phase Clock (TSPC) logic. It consists of three p-channel Metal-Oxide-Semiconductor (pMOS) and five n-channel Metal-Oxide-Semiconductor (nMOS) transistors. The schematic of PFD with DET-DFF is shown in Fig. 4. The outputs "UP" and "DOWN" are taken from both DFFs, whose inputs are connected to logic "1". The terminal "D" denotes the input signal while terminal "CLK" represents the clock signal. The proposed work involves using low-power techniques and together as a hybrid approach on the PFD circuit to reduce the power consumption. LECTOR, AVLS and stack techniques are chosen due to their minimal complexity and effectiveness.

The LECTOR technique focuses on reducing leakage power reduction. The circuit consists of one pMOS Field Effect Transistor (pMOSFET) and one nMOS Field Effect Transistor (nMOSFET) as Leakage Control Transistors (LCT). The LCT is stacked between the pull up and pull-down networks of the CMOS layout as shown in Fig. 3. The gate of nMOS is connected to the source of pMOS and the gate of pMOS is connected to the source of nMOS [10]. Due to this configuration, the nMOS is operated in cut-off when input is logic "1" and pMOS is operated in cut-off when input is logic "0", thereby reducing the leakage current and consequently the leakage power as well. The inputs are

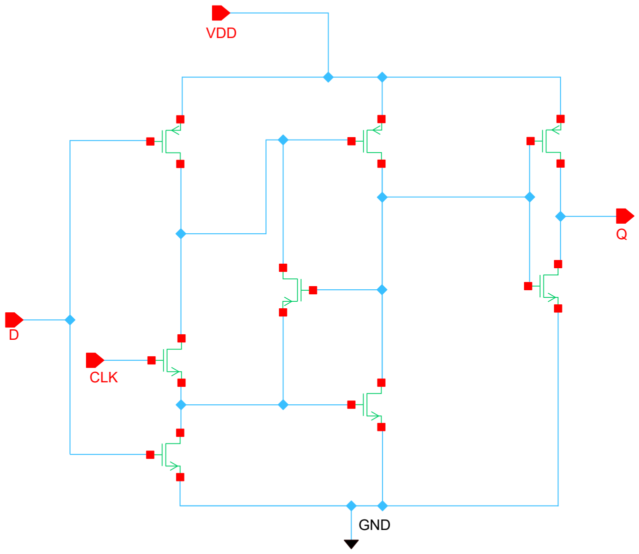

Fig. 3: Schematic of DET-DFF using TSPC logic.

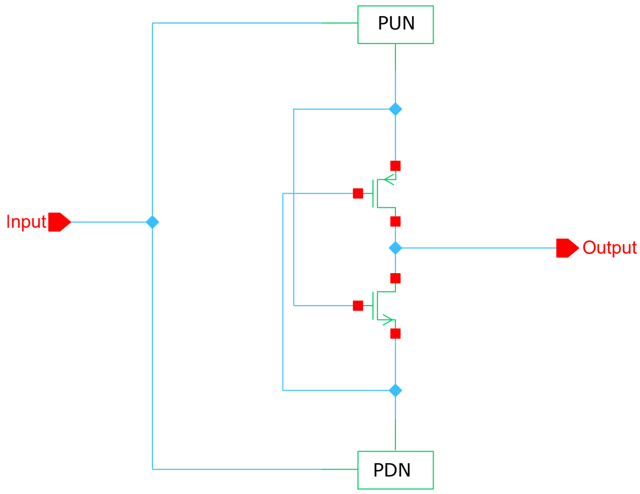

Fig. 5: A generic CMOS circuit with LECTOR technique.

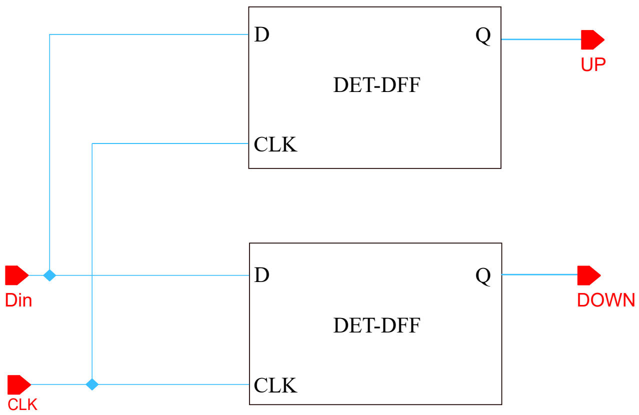

Fig. 4: Schematic of PFD realized using DET-DFF.

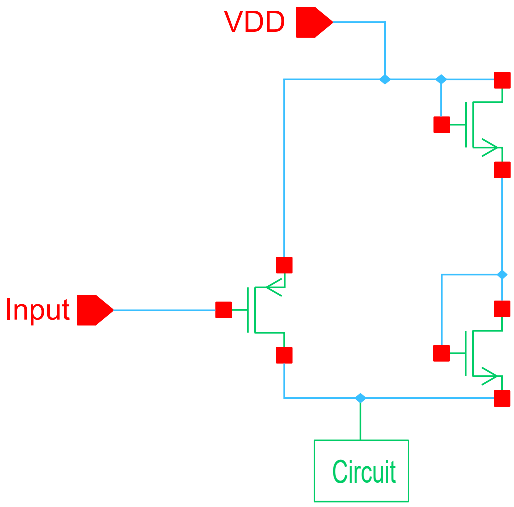

Fig. 6: Basic circuit illustrating AVLS.

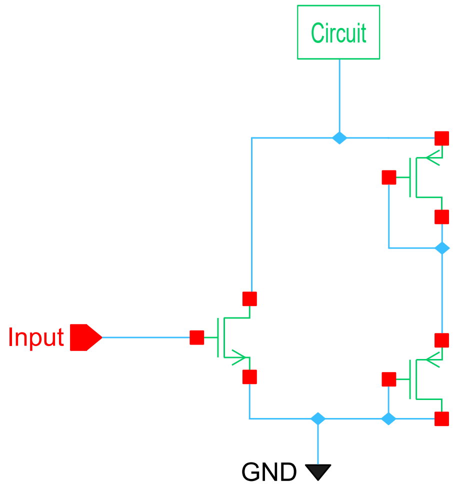

Fig. 7: Basic circuit illustrating AVLG.

given to both pull up and pull down as usual and the output is taken between stacked LCTs. The schematic of CMOS circuit with low-power LECTOR technique incorporated is as shown in Fig. 5.

AVL is a power reduction technique used in transistor level implementation of circuits. AVL can be incorporated in one of the two ways, one, AVL at Ground (AVLG), and another, AVL at Source (AVLS) [6] and [17]. AVLS and AVLG circuit representations are shown in Fig. 6 and Fig. 7. AVLS has one pMOS and two nMOS and AVLG has vice-versa. AVLS is connected between the circuit and the source voltage and AVLG is connected between the circuit and the ground potential. The gate of pMOS and nMOS in AVLS and AVLG are controlled by control input which is the clock signal of the circuit. They reduce the source voltage and increase the ground level voltage in AVLS and AVLG, respectively.

In either approach, the total voltage consumed by the circuit is reduced, thereby reducing the total power consumption. Using AVLS and AVLG together interferes with the working of the circuit as it reduces the total voltage by a huge factor, therefore it should be avoided. In the proposed work, AVLS is implemented over AVLG [17] as scaling down the supply voltage is more efficient compared to scaling up the ground level voltage.

The stack technique involves replacing the existing transistors with half the width of transistors [10]. They increase the circuit area by two-fold. The schematic of stack technique incorporation in a CMOS inverter is illustrated in Fig. 8. The use of a lesser width transistor increases the overall resistance to the leakage current path. Thus, when the circuit is unused, the leakage current is also reduced thereby reducing the static power consumption of the circuit.

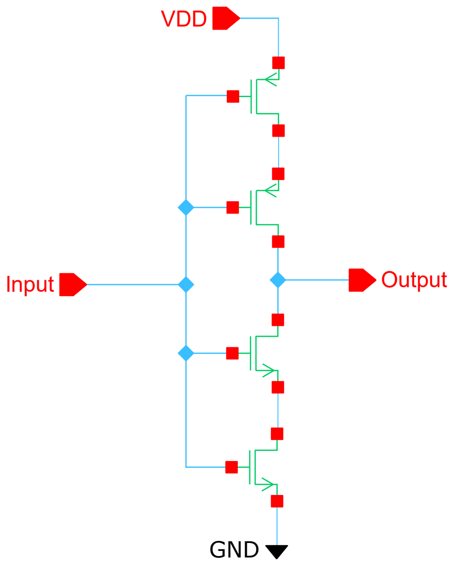

Fig. 8: Schematic of CMOS inverter with stack technique.

DET-DFF with the low-power LECTOR technique incorporated is shown in Fig. 9. The transistor count increases by one pMOS and nMOS. The pull up and pull-down circuits are separated at the last stage and pMOS and nMOS are stacked in between and output is taken from between them. Thus, when the circuit is unused, the leakage current from the last stage from where output is usually considered is now minimized by reducing power consumption.

Figure 10 illustrates the schematic of DET-DFF with AVLS incorporated. The AVLS uses the clock as a control signal and it reduces the source voltage. This reduced source voltage is now used as the new source voltage for the circuit, which reduces the total power consumption of the circuit. Figure 11 illustrates the schematic of DET-DFF with stack. As the transistors are replaced with half the width of transistors, the transistor count doubles. The transistor count increases by 100 %. A hybrid approach was taken with these techniques.

A hybrid low-power approach is derived by combining AVLS together with LECTOR and stack techniques. AVLS does not have an impact on the working of the circuit but simply alters the voltage level. Circuits of hybrid (AVLS and LECTOR techniques and AVLS and stack techniques) are illustrated in Fig. 12 and Fig. 13, respectively. In the proposed work, the hybrid low-power approach of AVLS and LECTOR is preferred over AVLS and stack techniques as the area occupied by the later circuit is considerably high whilst the power reduction from AVLS technique is insignificant.

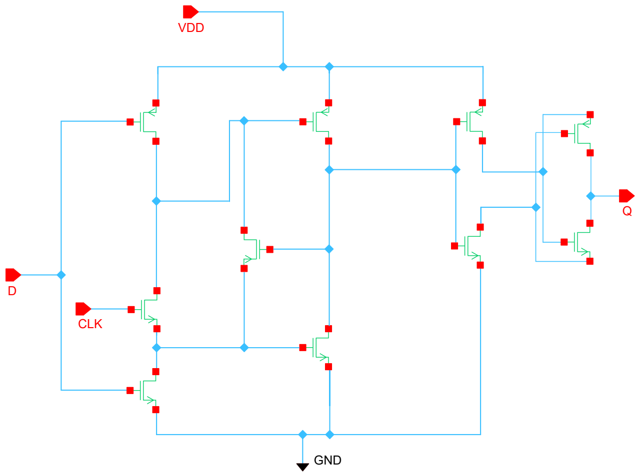

Fig. 9: Proposed circuit of DET-DFF with LECTOR technique.

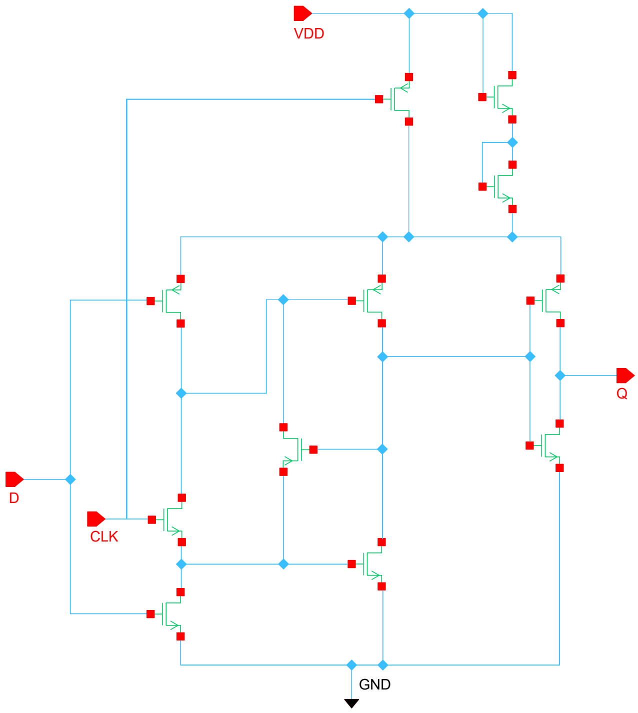

Fig. 10: Proposed circuit of DET-DFF with AVLS incorporated.

The low-power PFD has been implemented using two DET-DFFs. AVLS and LECTOR techniques are incor-

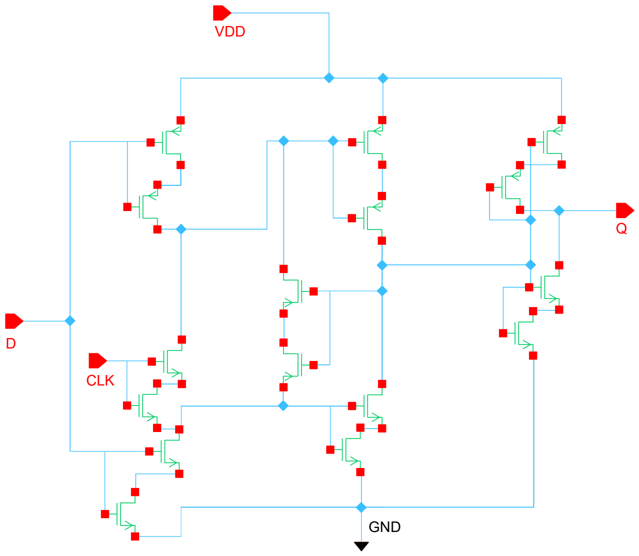

Fig. 11: Proposed circuit of DET-DFF with stack technique incorporated.

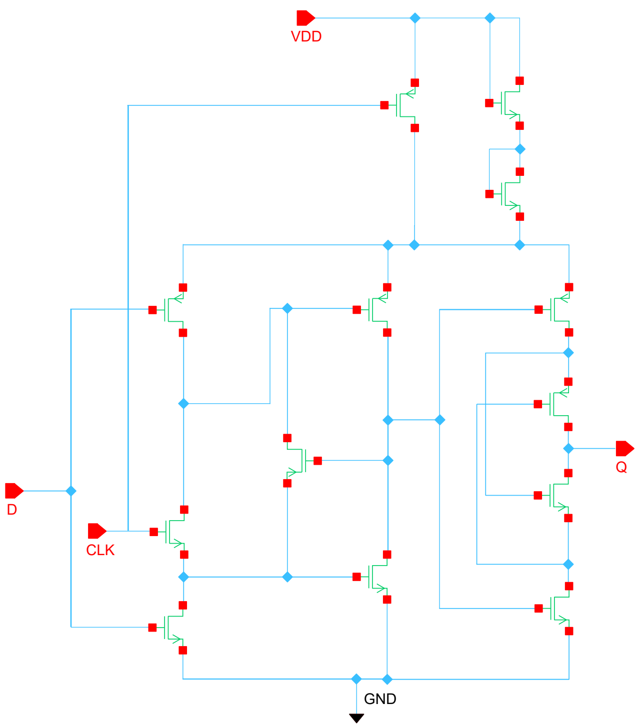

Fig. 12: DET-DFF with AVLS and LECTOR techniques incorporated.

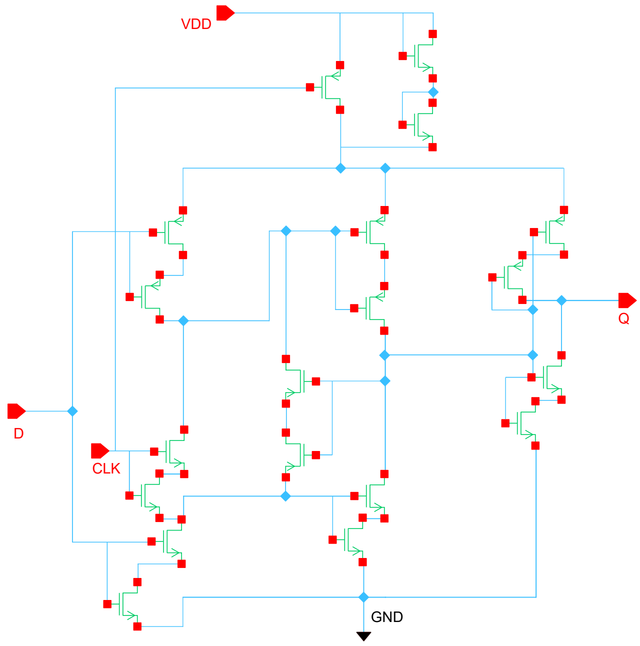

Fig. 13: DET-DFF with AVLS and stack techniques incorporated.

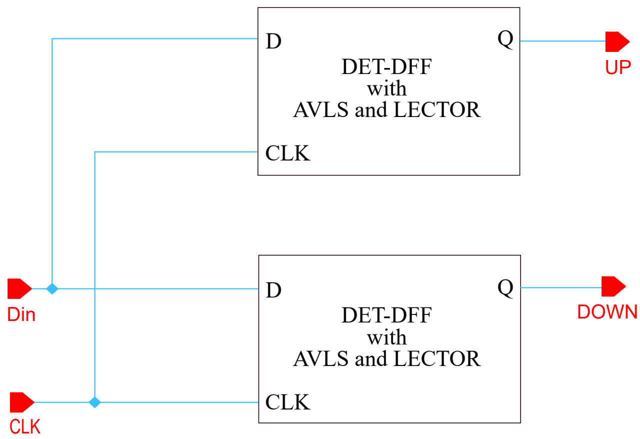

Fig. 14: PFD with AVLS and LECTOR techniques incorporated.

porated into the existing PFD architecture to reduce the power consumption along with the hybrid combination as well. Figure 14 shows the block diagram of PFD implemented using the DET-DFF with LECTOR and AVLS techniques incorporated. The proposed circuit is also realized in CMOS 90 nm technology for power, delay, and power delay product analysis.

4. Simulation and Results

Various low-power PFD architectures discussed in Sec. 3. have been designed and realized in Cadence Virtuoso in CMOS 180 nm and 90 nm Generic Process Design Kits (GPDK) technology. Simulations and power analysis have been performed in Cadence Spectre. In the circuits realized, bulk terminals of MOSFETs are connected to their respective source terminals.

The source voltage was maintained at 1.8 V and was simulated for a frequency ranging from 1 to 100 MHz at discrete intervals. The evaluation parameters for the performance of the PFD architectures include transistor count and power consumption. Simulation was

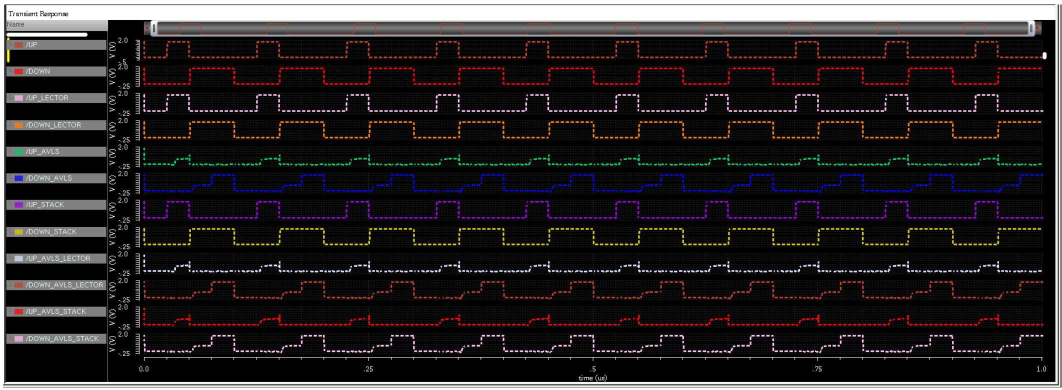

Fig. 15: Simulation analysis of proposed low-power PFD architecture at 20 MHz.

performed for frequencies through the range of 1 to 100 MHz. Figure 15 shows the simulation output waveforms of low-power PFD architectures using DET-DFF at 20 MHz operating frequency. The inputs for the circuit are "D" and "CLK". The signals "UP" and "DOWN" represent the outputs of PFD with DET-DFF. The remaining outputs are titled based on the type of low-power architecture that has been used. The outputs of LECTOR and stack techniques incorporated have fewer distortions compared to AVLS. Outputs of LECTOR and stack techniques are rectangular and do not deviate from the usual working of PFD. They have both strong logic "1" and "0" outputs as LECTOR and stack do not alter the source voltage.

The output of AVLS is not rectangular and has a weak logic "1" output. The combination of AVLS and LECTOR and AVLS and stack also follow the similar properties. If the application circuit has a threshold voltage beyond the capacity of the PLL, an external amplifier might be needed to improve the quality of output. The proposed PFD circuits are analyzed based on the merits of area occupied (in terms of transistor count) and the total power consumption.

Table 1 lists the number of MOSFETs used in the PFD architectures, including [8], [9] and PFD [1] and the area occupied in terms of transistor count for nMOS and pMOS. Proposed PFD designed to reduce the power consumption and the area occupied w.r.t. PFDs in [1], [8] and [9]. PFD with AVLS and LECTOR techniques requires minimal increase in area over [1] with the advantage of being low power.

The transistor counts for stack and the combination of AVLS, and stack increases by a factor of 2 and 2.13. Since the transistor area increases twice, these techniques are not considered for further power analysis. Power analysis has been performed for the proposed work through 1 to 100 MHz frequency range.

Table 2 shows the power consumed by various PFD architectures. For comparison, power consumption has been tabulated at 20 MHz. The PFD [9] consumes

Tab. 1: Transistor count of different PFD architectures.

PFD architectures	Transistor count	
	pMOS	nMOS
PFD [9]	35	35
PFD [8]	24	24
PFD [1]	8	8
PFD with AVLS	9	10
PFD with LECTOR	10	10
PFD with stack	16	16
PFD with AVLS and LECTOR	11	12
PFD with AVLS and stack	17	18

31.01 μW and the PFD [8] consumes 19 μW. PFD [1] with DET-DFF architecture without low-power consumes 4.65 μW of power. In comparison to [1], incorporating the LECTOR technique reduced the power consumption by 25.86 % and AVLS technique reduces power by 29.03 % respectively. The proposed hybrid architecture (incorporating LECTOR and AVLS) improves the efficiency by further reducing the power consumption to 32.47 % compared to PFD in [1]. The proposed PFD reduces power consumption by 83.47 % and 89.87 % over PFDs in [8] and [9] respectively, at 20 MHz frequency. The PFD architecture with AVLS and LECTOR has been also realized and simulated in 90 nm technology as well for comparison of the power delay product.

Tab. 2: Power analysis of low-power PFD architectures at 20 MHz.

PFD circuits	Power (μW)
PFD [9]	31.01
PFD [8]	19
PFD [1]	4.65
PFD with LECTOR	3.45
PFD with AVLS	3.3
PFD with AVLS and LECTOR	3.14

Table 3 shows the comparison between the power delay product of PFD in [1] and proposed PFD with AVLS and LECTOR techniques incorporated in CMOS 180 nm and 90 nm technology at 20 MHz frequency.

Tab. 3: Power delay product of proposed PFD with AVLS and LECTOR incorporation in 90 nm and 180 nm technology.

Proposed PFD circuits	Technology	Power (μW)	Delay (ps)	Power delay product
PFD [1]	180 nm	4.65	361	1660.6
PFD with AVLS and LECTOR	180 nm	3.14	346	1086.45
PFD with AVLS and LECTOR	90 nm	1.214	337	409.12

The power consumption using the 90 nm reduces the power consumption by 61.33 % in comparison to the 180 nm technology. Figure 16 shows the power consumption of PFD architectures over a range of frequencies from 1 to 100 MHz. The power comparison has been done with respect to PFD circuit in [1], which utilizes DET-DFF PFD architecture. There is a significant reduction in power compared to [1] by using the low-power techniques throughout the range. The trend seen over the frequency range is linear. As the frequency of operation increases, the percentage of power reduction also increases, showing that the low-power techniques and hybrid approach are highly effective in the higher frequency range, which is where a PLL is operated.

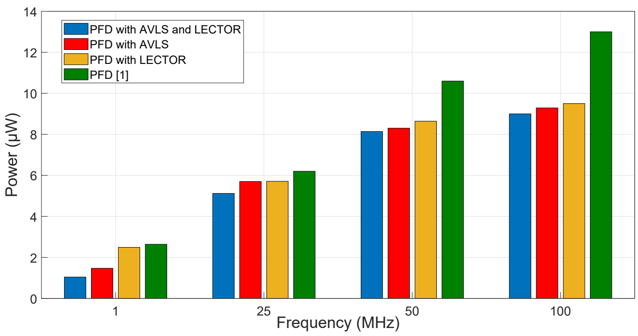

Fig. 16: Power of PFD architectures through range 1 to 100 MHz.

For instance, at input frequency of 20 MHz, proposed PFDs have a power reduction of 26 % achieved by using LECTOR and 29 % by using AVLS. The combination of both yields a reduction of up to 32 % when compared to PFD in [1]. Since area occupied was the first merit considered, based on which stack technique was not considered for the power analysis, further area optimization cannot be performed, as the PFD needs an external low-power technique which increases the area. As the voltage level is manipulated using AVLS, the circuit might require additional area for an external amplifier for voltage critical applications.

5. Conclusion and Future Research

PLL is an important circuit in communication systems whose efficiency depends largely on the individual parameters of PFD. The proposed PFD circuits demonstrate a reduction in power for a minimal increase in area. The AVLS technique shows a power reduction of 29 % for a 37.5 % increase in area; whilst the LECTOR offers a 25.8 % power reduction for just 25 % increase in area when compared to PFD [1]. The PFD with hybrid low-power techniques incorporated shows a power reduction of 32 % over PFD in [1]. Circuits wherein the area constraint is minimal, LECTOR or AVLS or the hybrid techniques can be used, thereby reducing the power output and increasing the overall circuit efficiency. Stacking of transistors is also an effective technique with the downside of increase in transistor area by two-fold. As AVLS affects the voltage level, the hybrid approach is limited to using only two techniques at once. The power consumption of PLL can be reduced by introducing a proposed low-power PFD. In comparison to the 180 nm technology, the 90 nm technology reduces the total power consumption by 61.33 %. For future work, other low-power approaches such as clock gating, variable level thresholds, and sleep transistors can be explored. A combination of three or even more low-power techniques can be analyzed to further optimize the circuit analysis without compromising on the output quality.

Author Contributions

The problem statement, design steps and analysis were contributed by B.S.P. Review of literature available; design methodology and implementation were contributed by S.S. Both the authors were involved in simulation. Results were obtained and inferences were derived by both the authors. Both the authors were involved in drafting the paper from initial stages, editing and revising the same.

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